Claims

1. An apparatus, comprising a bus controller adapted to provide virtual-to-physical address translation.

2. The apparatus of claim 1, wherein the bus controller comprises a table walk device to provide the virtual-to-physical address translation by performing a table walk to generate a physical address.

3. The apparatus of claim 2, further comprising a translation lookaside buffer (TLB) coupled to the bus controller to receive the physical address.

4. The apparatus of claim 1, wherein the bus controller comprises a table base register adapted to store a table base address.

5. The apparatus of claim 1, wherein the bus controller generates a read signal and a write signal, wherein the read signal indicates a read bus cycle is in progress and the write signal indicates that a write bus cycle is in progress.

6. The apparatus of claim 1, further comprising:

a memory device coupled to the bus controller; and

a processor coupled to the bus controller.

7. The apparatus of claim 6, wherein the bus controller is adapted to provide memory access protection.

8. The apparatus of claim 7, wherein the bus controller provides memory access protection by determining whether a process executing in the processor is permitted to access data stored in the memory device.

9. The apparatus of claim 8, wherein the bus controller transmits an abort signal to the processor when the process executing in the processor is not permitted to access data stored in the memory.

10. The apparatus of claim 6, wherein the processor operates at a first clock rate and the bus controller operates at a second clock rate, wherein the first clock rate is greater than the second clock rate.

11. The apparatus of claim 6, wherein the bus controller is adapted to provide control signals to the memory device.

12. The apparatus of claim 6, wherein the memory device is a nonvolatile memory device and the bus controller controls programming of the memory device.

13. The apparatus of claim 6, wherein the memory device is a volatile memory device and the bus controller controls refreshing of the memory device.

14. An apparatus, comprising:

a memory controller; and

a table walk device connected to the memory controller.

15. The apparatus of claim 14, wherein the table walk device combines a portion of a virtual address and a portion of a base address.

16. The apparatus of claim 14, wherein the table walk device comprises a table base register to store a table base address.

17. The apparatus of claim 14, further comprising a translation lookaside buffer (TLB) coupled to the table walk device.

18. The apparatus of claim 17, wherein the table walk device generates a descriptor and the TLB is adapted to receive the descriptor from the table walk device.

19. The apparatus of claim 14, wherein the table walk device is adapted to receive memory access protection data.

20. The apparatus of claim 14, wherein the apparatus further comprises:

a processor coupled to the table walk device; and

a memory device coupled to the memory controller.

21. The apparatus of claim 20, wherein the table walk device is adapted to determine whether a process executing in the processor is permitted to access data stored in the memory device.

22. The apparatus of claim 21, wherein the table walk device transmits an abort signal to the processor if the process is not permitted to access data stored in the memory device.

23. A system, comprising:

a processor;

a discrete memory controller adapted to perform a table walk operation and coupled to the processor; and

a volatile memory device coupled to the discrete memory controller.

24. The system of claim 23, further comprising a memory

management unit (MMU), wherein the discrete memory controller is coupled to the processor via the MMU.

25. The system of claim 24, wherein the MMU is adapted to provide memory access protection by preventing a process executing in the processor from accessing predetermined data in the volatile memory device.

26. The system of claim 23, wherein the discrete memory controller is adapted to provide address translation by using results of the table walk.

27. The system of claim 23, wherein the discrete memory controller performs a table walk by combining a portion of a virtual address and a portion of a base address to generate an address of a descriptor.

28. The system of claim 23, wherein the volatile memory device is a dynamic random access memory (DRAM) device.

29. A method, comprising:

executing instructions at a first clock rate; and

performing a table walk operation at a second clock rate.

30. The method of claim 29, wherein the first clock rate is

greater than the second clock rate.

31. The method of claim 29, further comprising determining memory access permission at the second clock rate.

32. The method of claim 29, wherein performing the table walk operation comprises concatenating a portion of a virtual address and a portion of a base address.

33. The method of claim 29, wherein performing the table walk operation comprises generating a descriptor.